Claims

What is claimed is:

[c1] An interface between memory and an integrated circuit, comprising:

a write path comprising a write data path and a forwarded clock path; and

a read path comprising a read data path,

wherein data propagated through the write path and read path is synchronized by a clock signal.

[c2] The interface of claim 1, wherein the write data path synchronizes operations with the forwarded clock path, and wherein the forwarded clock path and read data path use the clock signal as a time reference.

[c3] The interface of claim 1, wherein the clock signal is provided by the integrated circuit.

[c4] The interface of claim 1, wherein the read path and write path operatively connect the memory and the integrated circuit.

[c5] The interface of claim 1, wherein the memory is SDRAM.

[c6] The interface of claim 1, wherein the integrated circuit comprises a texture engine.

[c7] The interface of claim 1, wherein the write data path comprises circuitry having a first data propagation time, wherein the forwarded clock path comprises circuitry having a second data propagation time, and wherein the first data propagation time is substantially equal to the second data propagation time.

[c8] The interface of claim 1, wherein the read data path comprises:

pipeline circuitry adapted to compensate for accumulated phase generated by data propagation through the read data path.

[c9] The interface of claim 8, wherein the pipeline circuitry inputs at least one clock signal, and wherein the at least one clock signal is dependent on the clock signal.

[c10] A computer system having an interface dependent on a clock signal and having a write path and a read path comprising:

a memory, and

an integrated circuit,

wherein the interface operatively connects the memory and integrated circuit, synchronizes write data propagating through the write path with a first clock signal propagating through the write data path, and synchronizes read data propagating through the read path with a second clock signal.

[c11] The computer system of claim 10, wherein the first clock signal is derived from the second clock signal.

[c12] A method for synchronizing data propagation through an interface connecting memory and an integrated circuit, the interface having a write path and a read path, comprising:

propagating data through a write data path, wherein the write path comprises the write data path and a forwarded clock path;

propagating a clock signal through the forwarded clock path;

synchronizing the data propagation through the write data path to the forwarded clock path;

propagating data through a read data path, wherein the read path comprises the read data path; and

synchronizing the data propagation through the read data path to the clock signal.

[c13] The method of claim 12, wherein the clock signal is received from the integrated

circuit.

[c14] The method of claim 12, wherein the memory is SDRAM.

[c15] The method of claim 12, wherein the integrated circuit comprises a texture engine.

[c16] The method of claim 12, wherein the read path and write path operatively connect the memory and the integrated circuit.

[c17] The method of claim 12, wherein a first amount of delay is needed to propagate a first amount of data through the write data path, wherein a second amount of delay is needed to propagate a second amount of data through the forwarded clock path, and wherein the first amount of delay is substantially equal to the second amount of delay.

[c18] The method of claim 12, wherein synchronizing data propagation through the read data path to the clock signal comprises:

propagating read data through the read data path;

measuring accumulated phase of the read data relative to the clock signal; and

compensating for the accumulated phase.